Electronic Version
Stylesheet Version v1.1.1

METHOD FOR DESIGNING AN INTEGRATED CIRCUIT HAVINGMULTIPLE VOLTAGE DOMAINS

Abstract

A method for designing an integrated circuit having multiple voltage domains, including: (a) generating a logical integrated circuit design from information contained in a high-level design file, the high-level design file defining global connection declarations and voltage domain connection declarations; (b) synthesizing the logical integrated circuit design into a synthesized integrated circuit design based upon the logical integrated circuit design, information in a preferred components file and information in a voltage domain definition file; (c) generating a noise model from the synthesized integrated circuit design based on information in the voltage domain definition file and a design constraint file; and (d) simulating the noise model against constraints in the design constraint file and constraints in a circuit level profile file to determine if the synthesized integrated circuit design meets predetermined noise simulation targets.